AMENDMENTS TO THE CLAIMS

The claims in this listing will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A video signal conversion device for converting an input video signal to a video signal suitable for ~~to~~ a display device that carries out matrix display, comprising:

a storage that stores ~~part storing the~~ said input video signal as data;

a vertical frequency conversion processor that outputs ~~processing circuit outputting~~ a write control signal for writing ~~the~~ said input video signal in said storage ~~part~~ and a read control signal for reading the video signal stored in said storage to control ~~part to said storage part for controlling~~ input/output of the video signal in/from said storage ~~part~~ while converting the vertical frequency of the video signal by use of data stored in said storage ~~part~~;

an interlace-to-progressive conversion processor that converts ~~processing circuit converting~~, when the video signal output from said vertical frequency conversion ~~processing circuit~~ processor is an interlace signal, the video signal from the interlace signal to a progressive signal and outputs the progressive signal;

a scanning line conversion processor that converts ~~processing circuit converting~~ the number of scanning lines of the video signal output from said interlace-to-progressive conversion processor ~~processing circuit~~;

a horizontal pixel conversion processor that converts ~~processing circuit converting~~ the number of horizontal pixels of the video signal output from said scanning line conversion processor ~~processing circuit~~; and

a synchronous controller that outputs ~~control circuit outputting~~ a synchronous control signal to ~~for controlling operations of~~ said vertical frequency conversion processor ~~processing circuit~~, said interlace-to-progressive conversion processor ~~processing circuit~~, said scanning line conversion processor, ~~processing circuit~~ and said horizontal pixel conversion processor ~~processing circuit to~~ said synchronous control signal controlling operations of said vertical frequency conversion processor ~~processing circuit~~, said interlace-to-progressive conversion processor ~~processing circuit~~, said scanning line conversion processor, ~~processing circuit~~ and said horizontal pixel conversion processor ~~processing circuit~~,

wherein said input video signal is stored once in said storage to carry out vertical frequency conversion, interlace-to-progressive conversion, scanning line number conversion and horizontal pixel number conversion by use of the data stored in said storage.

2. (Currently Amended) The video signal conversion device according to claim 1, wherein

said storage ~~part~~ includes a field memory,

said vertical frequency conversion ~~processing circuit~~ processor includes:

a first line memory that performs ~~performing~~ a write operation with reference to a first clock output from said synchronous controller ~~control circuit~~ while performing a read operation with reference to a second clock output from said synchronous controller ~~control circuit~~ to perform write and read operations of said video signal in response to a horizontal synchronizing signal of a first system output from said synchronous controller ~~control circuit~~, and

said ~~a~~ vertical frequency conversion ~~processing circuit~~ processor operates ~~operating~~ with reference to said second clock for outputting said write control signal in response to said horizontal synchronizing signal of said first system and a vertical synchronizing signal of a first system output from said synchronous ~~control circuit~~ controller while outputting said read control signal in response to a horizontal synchronizing signal of a second system and a vertical synchronizing signal of a second system output from said synchronous ~~control circuit~~ controller to convert the vertical frequency of the video signal output from said first line memory from the frequency of said vertical synchronizing signal of said first system to the frequency of said vertical synchronizing signal of said second system,

said interlace-to-progressive conversion ~~processing circuit~~ processor includes:

a second line memory that operates ~~operating~~ with reference to said second clock for performing write and read operations of the video signal output from said vertical frequency conversion ~~processing circuit~~ processor in response to said horizontal synchronizing signal of said second system, and

an interlace-to-progressive ~~conversion circuit~~ converter operating with reference to said second clock for converting the video signal output from said second line memory from an interlace signal to a progressive signal in response to said horizontal synchronizing signal of said second system,

said scanning line conversion ~~processing circuit~~ processor includes:

a third line memory that operates ~~operating~~ with reference to said second clock to perform ~~for performing~~ a write operation of the video signal output from said interlace-to-progressive ~~conversion circuit~~ converter in response to said horizontal synchronizing signal of said second system while performing a read operation of the written video signal in response to a horizontal synchronizing signal of a third system output from said synchronous ~~control circuit~~ controller, and

a scanning line converter that operates ~~conversion circuit operating~~ with reference to said second clock for converting the number of scanning lines of the video signal output from said third line memory in response to said horizontal synchronizing signal of said third system and said vertical synchronizing signal of said second system, and

said horizontal pixel conversion ~~processing circuit~~ processor includes:

a horizontal compressor that operates ~~compression circuit operating~~ with reference to said second clock for compressing the number of horizontal pixels of the video signal output from said scanning line ~~conversion circuit~~ converter in response to said horizontal synchronizing signal of said third system,

a fourth line memory that performs ~~performing~~ a write operation with reference to said second clock while performing a read operation with reference to a third clock output from said synchronous ~~control circuit~~ controller to perform write and read operations of the video signal output from said horizontal compressor ~~compression circuit~~ in response to said horizontal synchronizing signal of said third system, and

a horizontal expander that operates ~~expansion circuit operating~~ with reference to said third clock for expanding the number of horizontal pixels of the video signal output from said fourth line memory in response to said horizontal synchronizing signal of said third system.

3. (Currently Amended) The video signal conversion device according to claim 1, wherein

said storage ~~part~~ includes a field memory, and

said interlace-to-progressive conversion ~~processing circuit~~ processor includes a plurality of line memories so that the video signal is transferred from said field memory to at least one of said plurality of line memories in response to a delayed horizontal synchronizing signal lagging a horizontal synchronizing signal before interlace-to-progressive conversion in phase, for performing rotation of data between said plurality of line memories while performing synthesis of an interpolation line with data of said plurality of line memories and reading data of a current line from a line memory other

than the line memory to which the video signal has been transferred among said plurality of line memories in response to said horizontal synchronizing signal.

4. (Currently Amended) The video signal conversion device according to claim 1, wherein

said storage ~~part~~ includes a field memory,

said vertical frequency conversion ~~processing circuit~~ processor includes:

an address generator that generates ~~generation circuit generating~~ a reading start address larger than a writing start address in ~~of~~ said field memory when increasing the number of scanning lines by said scanning line conversion ~~processing circuit~~ processor to perform ~~for performing~~ vertical expansion processing while generating a reading start address of a negative number when reducing the number of scanning lines by said scanning line conversion ~~processing circuit~~ processor to perform ~~for performing~~ vertical reduction processing, as the reading start address of said field memory, and

a black line inserter that inserts ~~insertion circuit inserting~~, when the reading start address of a negative number is generated by said address generator ~~generation circuit~~, data of a black line corresponding to a ~~by the~~ value of the negative number,

said synchronous ~~control circuit~~ controller includes a horizontal synchronizing signal generator that reduces ~~generation circuit reducing~~ the frequency of a horizontal synchronizing signal in reading of said field memory when performing said vertical expansion processing while increasing the frequency of the horizontal synchronizing

signal in reading of said field memory when performing said vertical reduction processing, and

said vertical frequency conversion ~~processing circuit~~ processor controls the read operation of said field memory in response to the horizontal synchronizing signal output from said horizontal synchronizing signal generator ~~generation circuit~~.

5. (Currently Amended) The video signal conversion device according to claim 1, wherein

said storage ~~part~~ includes a field memory,

said synchronous ~~control circuit~~ controller includes a determiner that determines ~~determination circuit determining~~ whether the video signal input in said vertical frequency conversion ~~processing circuit~~ processor is an odd field or an even field,

said vertical frequency conversion ~~processing circuit~~ processor includes a field information storage that stores ~~circuit storing~~ field information determined by said determiner ~~determination circuit~~ in response to a vertical synchronizing signal before vertical frequency conversion and reading the stored field information in linkage with the video signal stored in said field memory in response to the vertical synchronizing signal after vertical frequency conversion,

said vertical frequency conversion ~~processing circuit~~ processor outputs the video signal to said interlace-to-progressive ~~conversion circuit~~ converter in response to the field information read by said field information storage ~~circuit~~, and

said interlace-to-progressive conversion ~~processing circuit~~ processor converts the video signal output from said vertical frequency conversion ~~processing circuit~~ processor from an interlace signal to a progressive signal by intra-field interpolation.

6. (Currently Amended) The video signal conversion device according to claim 1, wherein

said synchronous ~~control circuit~~ controller includes:

a first horizontal synchronizing signal generator that generates ~~generation circuit generating a horizontal synchronizing signal for creating~~ a horizontal synchronizing signal forming the reference on the output side of said vertical frequency conversion ~~processing circuit~~ processor and on the input side of said scanning line conversion ~~processing circuit~~ processor,

a vertical synchronizing signal generator that generates ~~generation circuit generating~~ a vertical synchronizing signal with the horizontal synchronizing signal generated from said first horizontal synchronizing generator ~~generation circuit~~,

a second horizontal synchronizing signal generator that generates ~~generation circuit generating a horizontal synchronizing signal for creating~~ a horizontal synchronizing signal forming the reference on the output side of said scanning line conversion ~~processing circuit~~ processor, and

a selector that receives ~~selection circuit receiving~~ a vertical synchronizing signal created from a vertical synchronizing signal of the video signal input in said vertical

frequency conversion ~~processing circuit~~ processor and the vertical synchronizing signal output from said vertical synchronizing signal generator that selects and outputs ~~generation circuit for selecting and outputting~~ the vertical synchronizing signal of said vertical synchronizing signal generator ~~generation circuit~~ when said vertical frequency conversion ~~processing circuit~~ processor performs vertical frequency conversion while selecting and outputting the vertical synchronizing signal created from the vertical synchronizing signal of the video signal input in said vertical frequency conversion ~~processing circuit~~ processor when said vertical frequency conversion ~~processing circuit~~ processor performs no vertical frequency conversion as a vertical synchronizing signal for creating a vertical synchronizing signal forming the reference on the output side of said vertical frequency conversion ~~processing circuit~~ processor and forming the reference on the output side of said scanning line conversion ~~processing circuit~~ processor, and

said first and second horizontal synchronizing signal generators ~~generation circuits~~ are reset with reference to the vertical synchronizing signal output from said selector ~~selection circuit~~.

7. (Currently Amended) The video signal conversion device according to claim 6, wherein

said first horizontal synchronizing signal generator ~~generation circuit~~ includes a first counter that generates ~~generating~~ a horizontal synchronizing signal that creates ~~for creating~~ a horizontal synchronizing signal forming the reference on the output side of

said vertical frequency conversion ~~processing circuit~~ processor and on the input side of said scanning line conversion ~~processing circuit~~ processor,

said vertical synchronizing signal generator ~~generation circuit~~ includes a second counter dividing the frequency of the horizontal synchronizing signal generated from said first counter and generating a vertical synchronizing signal,

said second horizontal synchronizing signal generator ~~generation circuit~~ includes:

a third counter that generates ~~generating~~ a horizontal synchronizing signal for creating a horizontal synchronizing signal forming the reference on the output side of said scanning line conversion ~~processing circuit~~ processor while outputting said horizontal synchronizing signal as a reference pulse for a PLL circuit generating a prescribed clock, and

a fourth counter that decides ~~deciding~~ the dividing ratio of said PLL circuit, dividing the frequency of the clock output from said PLL circuit and generating a horizontal synchronizing signal that creates ~~for creating~~ a horizontal synchronizing signal forming the reference on the output side of said horizontal pixel conversion ~~processing circuit~~ processor, and

said first and third counters are reset with reference to the vertical synchronizing signal output from said selector ~~selection circuit~~.

8. (Currently Amended) The video signal conversion device according to claim 7, wherein

said fourth counter is reset with reference to the vertical synchronizing signal output from said selector ~~selection circuit~~.

9. (Currently Amended) A video signal conversion method for converting an input video signal to a video signal suitable for ~~to~~ a display device that carries out matrix display, with a storage that stores ~~part for storing~~ the video signal as data, ~~including~~ the method comprising:

outputting ~~a step of outputting~~ a write control signal for writing the input video signal in ~~said~~ the storage ~~part~~ and a read control signal for reading the video signal stored in ~~said~~ the storage ~~part to said storage part~~ and for controlling input/output of the video signal in/from ~~said~~ the storage ~~part~~ while converting the vertical frequency of the video signal by use of data stored in ~~said~~ the storage ~~part~~;

converting ~~a step of converting~~, when the video signal converted in ~~said~~ the vertical frequency conversion ~~step~~ is an interlace signal, the video signal from the interlace signal to a progressive signal and to output the progressive signal;

converting ~~a step of converting~~ the number of scanning lines of the video signal converted in ~~said~~ the interlace-to-progressive conversion ~~step~~;

converting ~~a step of converting~~ the number of horizontal pixels of the video signal converted in ~~said~~ the scanning line conversion; ~~step~~ and

generating ~~a step of generating~~ a synchronous control signal to synchronize the outputting and the converting ~~employed in respective said steps~~,

wherein the input video signal is stored once in the storage to carry out vertical frequency conversion, interlace-to-progressive conversion, scanning line number conversion, and horizontal pixel number conversion by use of the data stored in the storage.

10. (Currently Amended) The video signal conversion method according to claim 9, wherein ~~said~~ the storage ~~part~~ includes a field memory, ~~said~~ the vertical frequency conversion ~~step~~ includes:

performing ~~a step of performing~~ write and read operations of ~~said~~ the video signal in response to a horizontal synchronizing signal of a first system generated in ~~said~~ the synchronous control signal generation ~~step~~ with a first line memory performing a write operation with reference to a first clock generated in ~~said~~ the synchronous control signal generation ~~step~~ while performing a read operation with reference to a second clock generated in ~~said~~ the synchronous control signal generation ~~step~~, and

outputting ~~a step of outputting~~ ~~said~~ the write control signal in response to ~~said~~ the horizontal synchronizing signal of ~~said~~ the first system and a vertical synchronizing signal of a first system generated in ~~said~~ the synchronous control signal generation ~~step~~ while outputting ~~said~~ the read control signal in response to a horizontal synchronizing signal of a second system and a vertical synchronizing signal of a second system generated in ~~said~~ the synchronous control signal generation ~~step~~ with a vertical frequency converter ~~conversion circuit~~ operating with reference to ~~said~~ the second clock to convert

the vertical frequency of the video signal output from ~~said~~ the first line memory from the frequency of ~~said~~ the vertical synchronizing signal of ~~said~~ the first system to the frequency of ~~said~~ the vertical synchronizing signal of ~~said~~ the second system,

~~said~~ the interlace-to-progressive conversion ~~step~~ includes:

performing ~~a step of performing~~ write and read operations of the video signal output from ~~said~~ the vertical frequency converter ~~conversion circuit~~ in response to ~~said~~ the horizontal synchronizing signal of ~~said~~ the second system with a second line memory operating with reference to ~~said~~ the second clock, and

converting ~~a step of converting~~ the video signal output from ~~said~~ the second line memory from an interlace signal to a progressive signal in response to ~~said~~ the horizontal synchronizing signal of ~~said~~ the second system with an interlace-to-progressive converter ~~conversion circuit~~ operating with reference to ~~said~~ the second clock,

~~said~~ the scanning line conversion ~~step~~ includes:

performing ~~a step of performing~~ a write operation of the video signal output from ~~said~~ the interlace-to-progressive converter ~~conversion circuit~~ in response to ~~said~~ the horizontal synchronizing signal of ~~said~~ the second system while performing a read operation of the written video signal in response to a horizontal synchronizing signal of a third system generated in ~~said~~ the synchronous control signal generation ~~step~~ with a third line memory operating with reference to ~~said~~ the second clock, and

converting ~~a step of converting~~ the number of scanning lines of the video signal output from ~~said~~ the third line memory in response to ~~said~~ the horizontal synchronizing

signal of ~~said~~ the third system and ~~said~~ the vertical synchronizing signal of ~~said~~ the second system with a scanning line converter ~~conversion circuit~~ operating with reference to ~~said~~ the second clock, and

~~said~~ the horizontal pixel conversion ~~step~~ includes:

compressing ~~a step of compressing~~ the number of horizontal pixels of the video signal output from ~~said~~ the scanning line converter ~~conversion circuit~~ in response to ~~said~~ the horizontal synchronizing signal of ~~said~~ the third system with a horizontal compressor ~~compression circuit~~ operating with reference to ~~said~~ the second clock,

performing ~~a step of performing~~ write and read operations of the video signal output from ~~said~~ the horizontal compressor ~~compression circuit~~ in response to ~~said~~ the horizontal synchronizing signal of ~~said~~ the third system with a fourth line memory performing a write operation with reference to ~~said~~ the second clock while performing a read operation with reference to a third clock generated in ~~said~~ the synchronous control signal generation ~~step~~, and

expanding ~~a step of expanding~~ the number of horizontal pixels of the video signal output from ~~said~~ the fourth line memory in response to ~~said~~ the horizontal synchronizing signal of ~~said~~ the third system with a horizontal expander ~~expansion circuit~~ operating with reference to ~~said~~ the third clock.

11. (Currently Amended) The video signal conversion method according to claim 9, wherein

~~said~~ the storage ~~part~~ includes a field memory, and

~~said~~ the interlace-to-progressive conversion ~~step~~ includes ~~a step of~~ employing a plurality of line memories and transferring the video signal to at least one of ~~said~~ the plurality of line memories from ~~said~~ the field memory in response to a delayed horizontal synchronizing signal lagging a horizontal synchronizing signal before interlace-to-progressive conversion in phase for performing rotation of data between ~~said~~ the plurality of line memories while performing synthesis of an interpolation line with data of ~~said~~ the plurality of line memories for reading data of a current line from one line memory other than the line memory to which the video signal has been transferred among ~~said~~ the plurality of line memories in response to ~~said~~ the horizontal synchronizing signal.

12. (Currently Amended) The video signal conversion method according to claim 9, wherein

~~said~~ the storage ~~part~~ includes a field memory,

~~said~~ the vertical frequency conversion ~~step~~ includes:

generating ~~a step of generating~~ a reading start address larger than a writing start address of ~~said~~ the field memory when increasing the number of scanning lines in ~~said~~ the scanning line conversion, and ~~step~~ for performing vertical expansion processing while generating a reading start address of a negative number when reducing the number of scanning lines in ~~said~~ the scanning line conversion ~~step~~ for performing vertical reduction processing, as the reading start address of ~~said~~ the field memory, and

inserting ~~a step of inserting~~, when the reading start address of a negative number is generated in ~~said~~ the address generation ~~step~~, data of a black line corresponding to a ~~by the~~ value of ~~said~~ the negative number,

~~said~~ the synchronous control signal generation ~~step~~ includes ~~a step of~~ reducing a ~~the~~ frequency of a ~~the~~ horizontal synchronous signal in reading of ~~said~~ the field memory when performing ~~said~~ the vertical expansion processing while increasing the frequency of the horizontal synchronous ~~synchronizing~~ signal in reading of ~~said~~ the field memory when performing ~~said~~ the vertical reduction processing, and

~~said~~ the vertical frequency conversion ~~step~~ includes ~~a step of~~ controlling the read operation of ~~said~~ the field memory in response to the horizontal synchronizing signal output in ~~said~~ the synchronous control signal generation ~~step~~.

13. (Currently Amended) The video signal conversion method according to claim 9, wherein

~~said~~ the storage ~~part~~ includes a field memory,

~~said~~ the synchronous control signal generation ~~step~~ includes ~~a step of~~ determining whether the video signal input in ~~said~~ the vertical frequency conversion ~~step~~ is an odd field or an even field,

~~said~~ the vertical frequency conversion ~~step~~ includes ~~a step of~~ storing field information determined in ~~said~~ the determination ~~step~~ in response to a vertical synchronizing signal before vertical frequency conversion and reading the stored field

information in linkage with the video signal stored in ~~said~~ the field memory in response to the vertical synchronizing signal after vertical frequency conversion,

~~said~~ the vertical frequency conversion ~~step~~ includes ~~a step of~~ outputting the video signal in response to the read field information, and

~~said~~ the interlace-to-progressive conversion ~~step~~ includes ~~a step of~~ converting the video signal output in response to ~~said~~ the field information from an interlace signal to a progressive signal by intra-field interpolation.

14. (Currently Amended) The video signal conversion method according to claim 9, wherein

~~said~~ the synchronous control signal generation ~~step~~ includes:

generating ~~a step of generating a horizontal synchronizing signal for creating~~ a horizontal synchronizing signal forming the reference on the output side in ~~said~~ the vertical frequency conversion ~~step~~ and on the input side in ~~said~~ the scanning line conversion ~~step~~ with a first horizontal synchronizing signal generator ~~generation circuit~~,

generating ~~a step of generating~~ a vertical synchronizing signal with the horizontal synchronizing signal generated from ~~said~~ the first horizontal synchronizing signal generator ~~generation circuit~~ with a vertical synchronizing signal generator ~~generation circuit~~,

generating ~~a step of generating a horizontal synchronizing signal for creating~~ a horizontal synchronizing signal forming the reference on the output side in ~~said~~ the

scanning line conversion ~~step~~ with a second horizontal synchronizing signal generator ~~generation circuit~~,

receiving ~~a step of receiving~~ a vertical synchronizing signal created from a vertical synchronizing signal of the video signal on the input side in ~~said~~ the vertical frequency conversion ~~step~~ and the vertical synchronizing signal output from ~~said~~ the vertical synchronizing signal generator ~~generation circuit~~ for selecting and outputting the vertical synchronizing signal of ~~said~~ the vertical synchronizing signal generator ~~generation circuit~~ when performing vertical frequency conversion in ~~said~~ the vertical frequency conversion ~~step~~ while selecting and outputting the vertical synchronizing signal created from the vertical synchronizing signal of the video signal on the input side in ~~said~~ the vertical frequency conversion ~~step~~ when performing no vertical frequency conversion in ~~said~~ the vertical frequency conversion ~~step~~ as a vertical synchronizing signal for creating a vertical synchronizing signal form the reference on the output side in ~~said~~ the vertical frequency conversion ~~step~~ and forming the reference on the output side in ~~said~~ the scanning line conversion ~~step~~, and

resetting ~~a step of resetting said~~ the first and second horizontal synchronizing signal generators ~~generation circuits~~ with reference to the vertical synchronizing signal selected in ~~said~~ the selection ~~step~~.

15. (Currently Amended) The video signal conversion method according to claim 14, wherein

generating ~~said step of generating~~ the horizontal synchronizing signal with ~~said~~ the first horizontal synchronizing signal generator which ~~generation circuit~~ includes ~~a step of~~ generating a horizontal synchronizing signal for creating a horizontal synchronizing signal forming the reference on the output side in ~~said~~ the vertical frequency conversion ~~step~~ and on the input side in ~~said~~ the scanning line conversion ~~step~~ with a first counter,

generating ~~said step of generating~~ the vertical synchronizing signal with ~~said~~ the vertical synchronizing signal generator which ~~generation circuit~~ includes ~~a step of~~ dividing the frequency of the horizontal synchronizing signal generated from ~~said~~ the first counter and generating a vertical synchronizing signal with a second counter,

generating ~~said step of generating~~ the horizontal synchronizing signal with ~~said~~ the second horizontal synchronizing signal generator ~~generation circuit~~ includes:

generating ~~a step of generating~~ a horizontal synchronizing signal for creating a horizontal synchronizing signal forming the reference on the output side in ~~said~~ the scanning line conversion ~~step~~ while generating ~~said~~ the horizontal synchronizing signal as a reference pulse for a PLL circuit generating a prescribed clock with a third counter, and

deciding ~~a step of deciding~~ the dividing ratio of ~~said~~ the PLL circuit, dividing the frequency of the clock output from ~~said~~ the PLL circuit and generating a horizontal synchronizing signal for creating a horizontal synchronizing signal forming the reference on the output side in ~~said~~ the horizontal pixel conversion ~~step~~ with a fourth counter, and

resetting ~~said step of resetting said~~ the first and second horizontal synchronizing signal generator ~~generation circuits~~ includes ~~a step of~~ resetting the first and third counters with reference to the vertical synchronizing signal selected in ~~said~~ the selection ~~step~~.

16. (Currently Amended) The video signal conversion method according to claim 15, wherein

resetting ~~said step of resetting said~~ the first and second horizontal synchronizing signal generator ~~generation circuits~~ further includes ~~a step of~~ resetting ~~said~~ the fourth counter with reference to the vertical synchronizing signal selected in ~~said~~ the selection ~~step~~.